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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/750,589
Filing Date: December 31, 2003
Appellant(s): JIANG ET AL.

Timothy N. Trop
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 03 February 2009 appealing from the Office action mailed 11 June 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,951,672	Kwok et al.	9-1999
6,018,785	Wenniger	1-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12-21 and 26-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwok et al. (US Pat No. 5,951,672 hereinafter Kwok), in view of Wenniger (US Pat No. 6,018,785).

Claim 12

Kwok teaches an apparatus comprising:

execution circuitry to receive and execute a first thread of instructions corresponding to a first graphical element of an image and a second thread of instructions corresponding to a second graphical element of the image (Kwok Fig 5, wherein a main thread handles graphics work A and a child thread handles graphic works B), wherein the execution circuit places the first thread in an inactive state in response to the first thread requiring a resource having an associated semaphore (Kwok col 4 lines 35-44, wherein the first thread is placed in a waiting state after testing variables linking the two threads); and

a semaphore entity coupled with the execution circuitry (Kwok col 2 lines 11-15, 27-30), to selectively grant control of the semaphore, wherein the execution circuitry removes the thread of instructions from the inactive state (Kwok col 4 lines 35-44, wherein the task is executed).

Kwok does not explicitly teach that a semaphore request message is transmitted and that a semaphore acknowledge message is received from the semaphore entity. However, Wenniger teaches using an active semaphore as opposed to a passive semaphore to generate an interrupt signal or message that is sent to all requesting processes whenever a semaphore status changes (Wenniger col 6 lines 1-22). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kwok to use an active semaphore. One would be motivated by the desire to reduce unnecessary resource usage caused by continuous polling of passive semaphores as indicated by Wenniger (Wenniger col 6 lines 10-12).

Claim 13

Kwok teaches that the execution circuitry comprises: a first execution circuit to execute the first thread of instructions; and a second execution circuit to execute the second thread of instructions (Kwok col 1 lines 31-37, wherein multiple processors are available to execute multiple sub tasks)

Claim 14

Kwok and Wenniger do not explicitly teach that the first thread comprises a first set of ray tracing instructions and the first graphical element comprises a first ray segment, and further wherein the second thread comprises a second set of ray tracing instructions and the second graphical element comprises a second ray segment.

However, Kwok teaches that lighting and illumination are a crucial part of graphics processing (Kwok col 7 lines 31-48). It would have been obvious to one of ordinary skill at the time of the invention that the first thread comprises a first set of ray tracing instructions and the first graphical element comprises a first ray segment, and the second thread comprises a second set of ray tracing instructions and the second graphical element comprises a second ray segment since processing such graphical elements are commonly done by processors processing graphics..

Claims 15-16

Kwok and Wenniger do not teach that the first thread comprises a first set of video decoding instructions and the first graphical element comprises a first picture segment comprising a first macroblock, and further wherein the second thread comprises a second set of video decoding instructions and the second graphical element comprises a second picture segment comprising a second macroblock.

It would have been obvious to one of ordinary skill in the art at the time of the invention to include that the first and second thread process a set of video decoding instructions and graphical elements comprising macroblocks. One would be motivated by the desire to extend the scope of Kwok and Wenniger to video decoding.

Claim 17

Kwok and Wenniger do not explicitly teach that the first thread comprises a first set of three-dimensional rendering instructions and the first graphical element comprises a first render primitive, and further wherein the second thread comprises a second set of three-dimensional rendering instructions and the second graphical element comprises a second render primitive.

Kwok does teach that the processor must process three-dimensional primitives (Kwok col 5 lines 12-19). It would have been obvious to one of ordinary skill at the time of the invention that the first thread comprises a first set of three-dimensional rendering instructions and the first graphical element comprises a first render primitive, and further

wherein the second thread comprises a second set of three-dimensional rendering instructions and the second graphical element comprises a second render primitive since processing such graphical elements are commonly done by processors processing graphics.

Claim 18

Kwok and Wenniger do not explicitly teach that the first render primitive comprises one of a first point, a first line, a first triangle, and a first triangle strip, and further wherein the second render primitive comprises one of a second point, a second line, a second triangle, and a second triangle strip.

Kwok does teach that primitives are triangles defined by three vertices (Kwok col 5 lines 21-21). It would have been obvious to one of ordinary skill at the time of the invention that primitives comprise one of a point, a line, a triangle, and a triangle strip.

Claim 19

Kwok teaches further comprising a memory coupled with the execution circuitry to store the first thread of instructions and the second thread of instructions (wherein it is inherent that memory is used to store the instructions).

Claim 20

Kwok and Wenniger do not explicitly teach further comprising: at least one additional execution circuit to execute threads of instructions; and a thread dispatcher coupled with the execution circuitry and at least one additional execution circuit to dispatch threads for execution.

While Kwok already teaches multiple processors (Kwok col 1 lines 31-37, wherein multiple processors are available to execute multiple sub tasks), it would have been obvious to one of ordinary skill in the art, at the time of the invention to add one additional execution circuit to execute threads of instructions and a thread dispatcher. It is well known in the art to add additional execution units to increase processing capability of processors.

Claim 21

Regarding claim 21, Wenniger teaches that when the first thread of instructions is in the inactive state, execution of the instructions ceases and the execution circuitry does not poll the semaphore entity to determine a status of the semaphore request message (col 5 lines 12-16, wherein Process B awaits receipts of an interrupt from the semaphore).

Claims 26-34

They are the system claims of claims 12-21 above. Therefore, they are rejected for the same reasons as claims 12-21 above.

(10) Response to Argument

The cited prior art in question, Wenniger (US Pat No. 6,018,785), discloses the use of a hardware semaphore apparatus used for the synchronization of resource access by multiple processes (col 2 lines 11-37).

Appellant's arguments filed 03 February 2009 have been fully considered but they are not persuasive. Appellant argues that "the processor in Wenniger never places process B in an inactive state – process B just stops polling" (Brief: pg 10, section A (1)). This argument is not found to be persuasive in view of the cited prior art and Applicant's specification.

First, the claim language requires that a first thread be placed in an inactive state. Appellant argues that for a process to be placed in an inactive state, execution for that process must cease. However, such an interpretation of the term 'inactive' is too narrow in meaning. While it is entirely possible for process B in Wenniger to execute other tasks, the very fact that it stops polling indicates that it is inactive from a relative stand point.

Secondly, Applicant's specification gives a clear definition on what is meant by an inactive state. Applicant's specification recites, "after sending the semaphore request message, the requesting thread is placed in an inactive state in which execution and associated operations (e.g., polling of semaphores) halts" (Specification [0015]). Therefore, Applicant's own specification admits that halting the polling of the semaphore is an example of placing a thread in an inactive state.

Appellant further argues that "instead of just issuing an interrupt, which then causes the process B to have to check the resource's availability all over, the claimed semaphore entity grants the resource" (Brief: pg 10, section A (2)). This argument is not found to persuasive in view of the cited prior art and the claims.

First, the claimed semaphore entity does not necessarily grant the resource as the claim language recites "*selectively* grant control". Furthermore, independent claims 12 and 26 only require that "the execution circuitry, in response to receiving the semaphore acknowledge message, removes the thread of instructions from the inactive state". Therefore, there is no explicit granting of the resource as argued by Appellant; there is only the explicit step of removing the thread from the inactive state.

Secondly, Wenniger reads upon the above interpretation of the claims by teaching that requesting processes are again allowed to re-poll the semaphore upon receiving a message such as in interrupt (Wenniger col 6 lines 12-22, wherein process B may query the semaphore upon receipt of an interrupt). Therefore, Wenniger teaches an explicit step where processes that have polling halted (e.g. made inactive), are then allowed to poll once again (e.g. made active).

Appellant argues that "Thus, all in one step, control for the semaphore is granted and the thread is removed from the inactive state. Even if the Examiner were to argue that Wenniger somehow removes the thread from the inactive state, his argument that it is removed from the inactive state by enabling it to continue polling proves that the

thread was not granted control of the semaphore" (Brief: pg 11, section A). This argument is not found to persuasive in view of the cited prior and the claims.

First, Appellant's arguments are not consistent with the claimed language. The granting of the semaphore is not granted in one step since the claim recites multiple steps for granting control in which a semaphore acknowledge message must be sent, the acknowledge message must be received, and then the thread is removed from the inactive state. Furthermore, the claims leave it unclear as to which of the steps performs the actual granting of the resource since the end result only requires that the thread be removed from the inactive state. Therefore, the prior art meets the claim language as long as the prior art includes the granting of a semaphore which includes the steps of sending a message and removal of threads from an inactive state.

Secondly, contrary to Appellant's arguments, Wenniger is directed to allowing a thread to be granted control to a semaphore. It is clear from Wenniger's disclosure that control over the semaphore is granted eventually (Wenniger col 2 lines 32-37). Therefore, while it is true that Wenniger removes the thread from the inactive state by re-enabling polling, such re-polling leads to the granting control of the semaphore. Wenniger reads upon the claim language by selectively granting control of the semaphore by sending an interrupt to all requesting processes. All requesting processes receive the interrupt and re-poll. Control is selectively granted to the process that polls the semaphore first. It is clear such an interpretation reads upon the claims. Therefore, the rejections have been maintained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Eric C Wai/

Examiner, Art Unit 2195

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